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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ehlert et al.

Attorney Docket No.:
NSC1P202/P04892

Patent: 6,800,815 B1

Issued: October 5, 2004

Title: MATERIALS AND STRUCTURE FOR A HIGH RELIABILITY BGA CONNECTION BETWEEN LTCC AND PB BOARDS

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on November 17, 2004 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where they occur, and shown correctly in the application filed, are as follows:

SPECIFICATION:

1. Column 3, line 58, change "and toe portion" to --and the portion--. This appears correctly in the patent application as filed on page 5, line 30.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P202).

Respectfully submitted,
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DETAILED DESCRIPTION OF THE INVENTION

The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order to not unnecessarily obscure the present invention.

Generally, the present patent application discloses a structural design and a method for forming LTCC integrated circuit modules that exhibit long thermal cycle fatigue lives after being attached to electronic substrates, such as printed circuit boards. The present invention thereby greatly increases the utility and value of LTCC modules.

FIG. 2A is now presented to diagrammatically illustrate the structure of one possible embodiment of the present invention. FIG. 2A is a side plan, cross-sectional view of a portion of the bottom ceramic layer 202 of a multi-layered LTCC module 200. To provide an additional perspective view of the structure, FIG. 2B illustrates a top plan view of the bottom surface 212 of layer 202. As can be seen in FIG. 2A, a conductive trace 204, which is on the upper surface 201 of layer 202, is electrically connected to electrically conductive material within through-hole 206. Through-hole 206 is a passageway that passes through a substantial portion of the layer's thickness. The electrically conductive material within the through-hole 206 forms via 207. At the end of via 207, opposite conductive trace 204, is formed a catch pad 208. A conductive barrier cap 209 is formed in connection to catch pad 208. Barrier cap 209 forms an intermediate conductive material through which catch pad 209 is connected to the material forming contact (or solder) pad 210, which is formed on the bottom surface 212 of layer 202. Barrier cap 209 serves as a barrier that prevents chemical reactions from occurring between the material of via 207 and catch pad 208 with the material of contact pad 210. Layer 202 is typically the bottom layer of a laminate LTCC module. A ring of dielectric material 214 is formed on the bottom surface 212 of layer 202 such that the perimeter of the contact pad 210 and the portion of the ceramic layer 202 immediately surrounding the contact pad 210 is covered by the ring. Within the ring 214 and on the surface of the contact pad 210 is placed solder material 216. Solder 216 is used to attach the LTCC module 200 to an electronic substrate, such as a printed circuit board. It is common to use a lead/tin composite material for the solder material 216. Again, FIG. 2B illustrates a plan view of the bottom

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(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,800,815,B1

DATED : October 5, 2004

INVENTOR(S) : Ehlert et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Specifications:

Column 3, line 58, change "and toe portion" to --and the portion--.

MAILING ADDRESS OF SENDER:

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